

FIG. 1
(PRIOR ART)

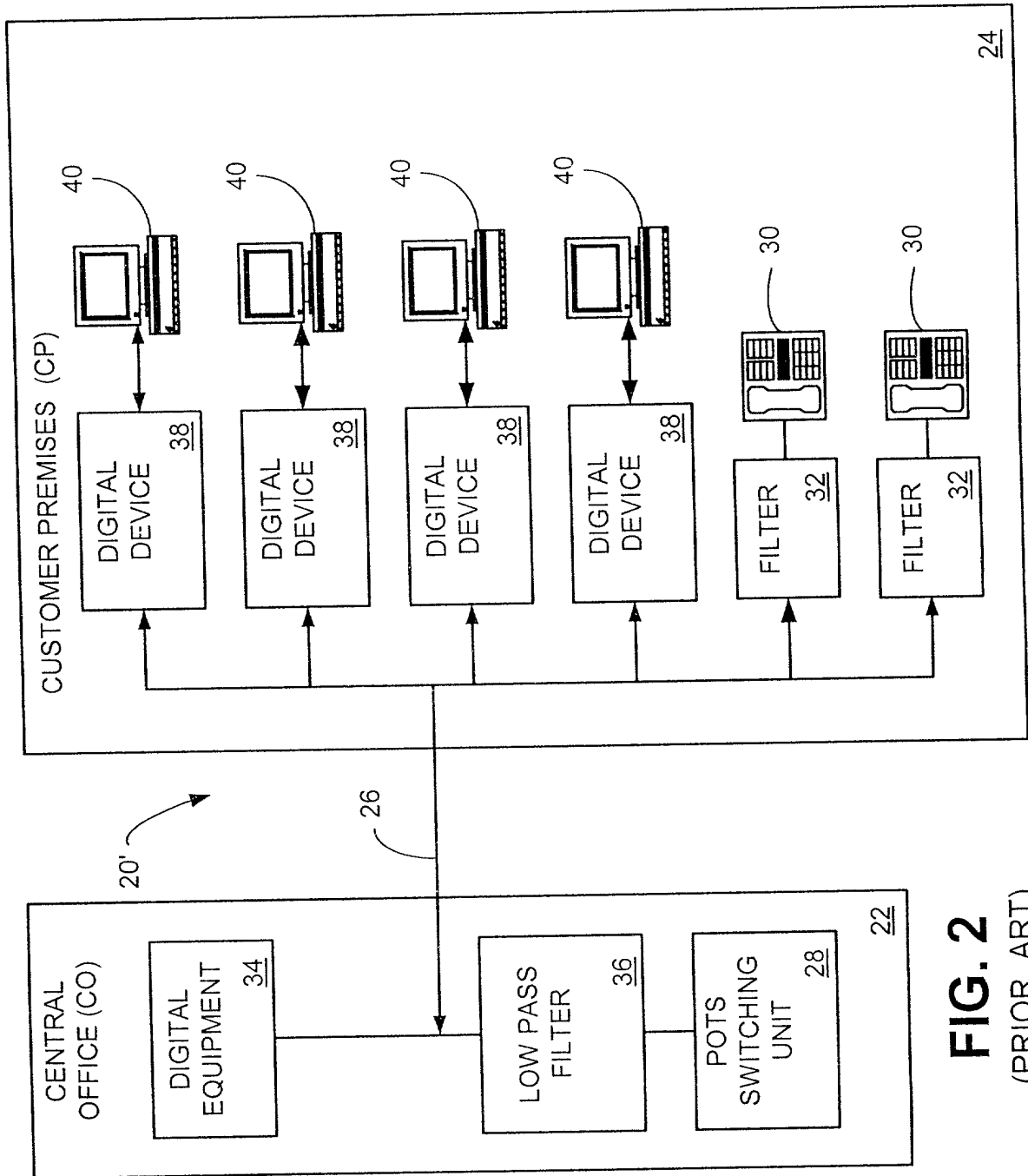
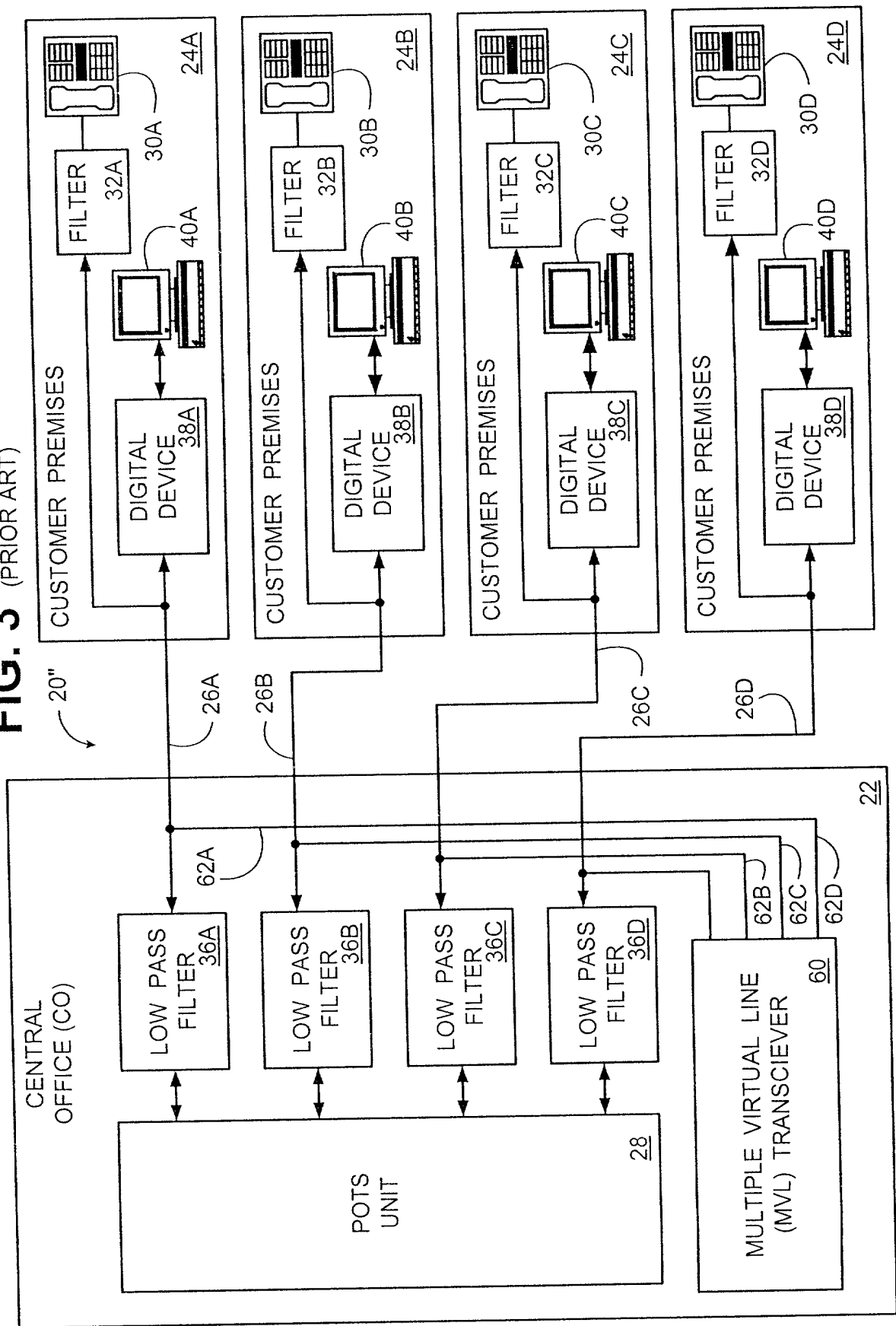


FIG. 2
(PRIOR ART)

FIG. 3 (PRIOR ART)



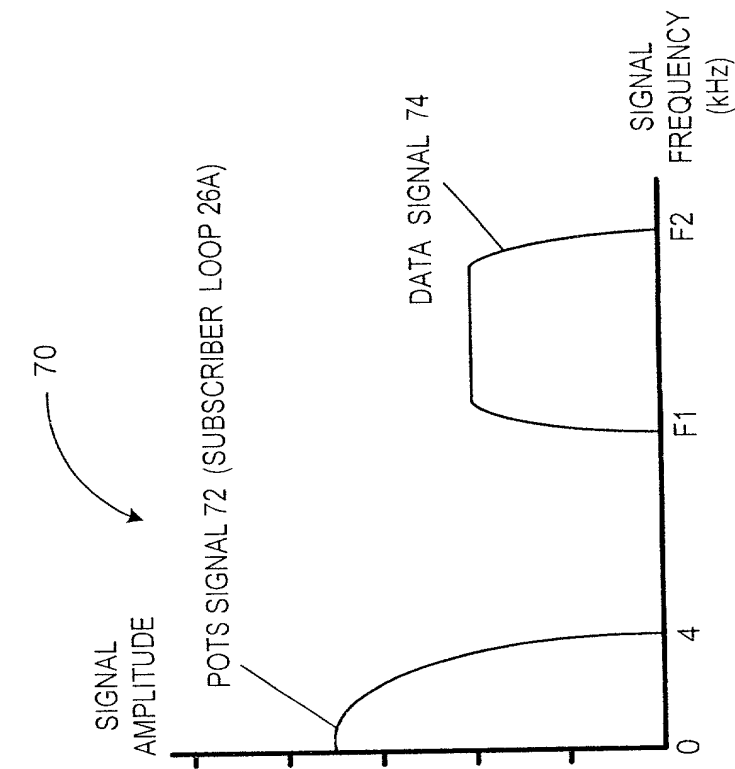


FIG. 4A
(PRIOR ART)

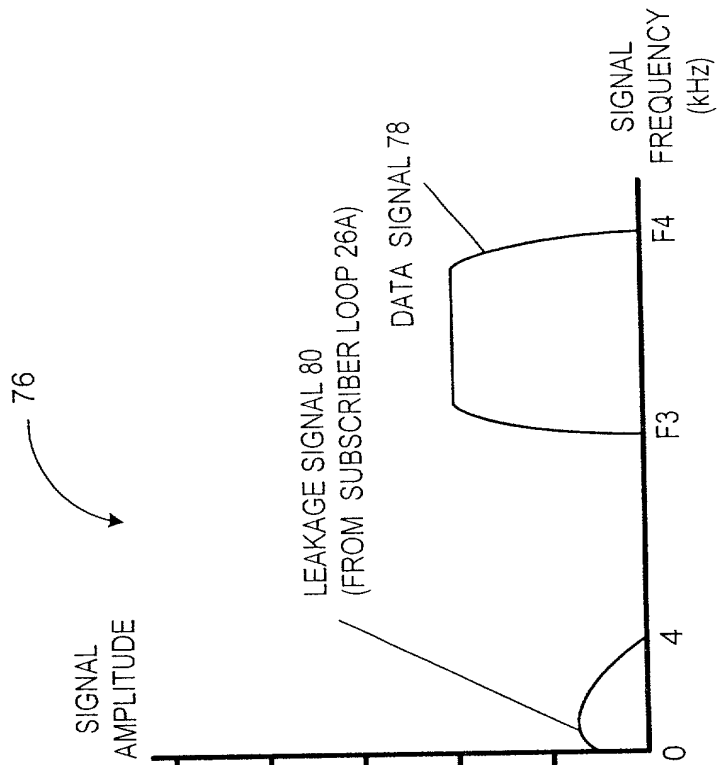


FIG. 4B
(PRIOR ART)

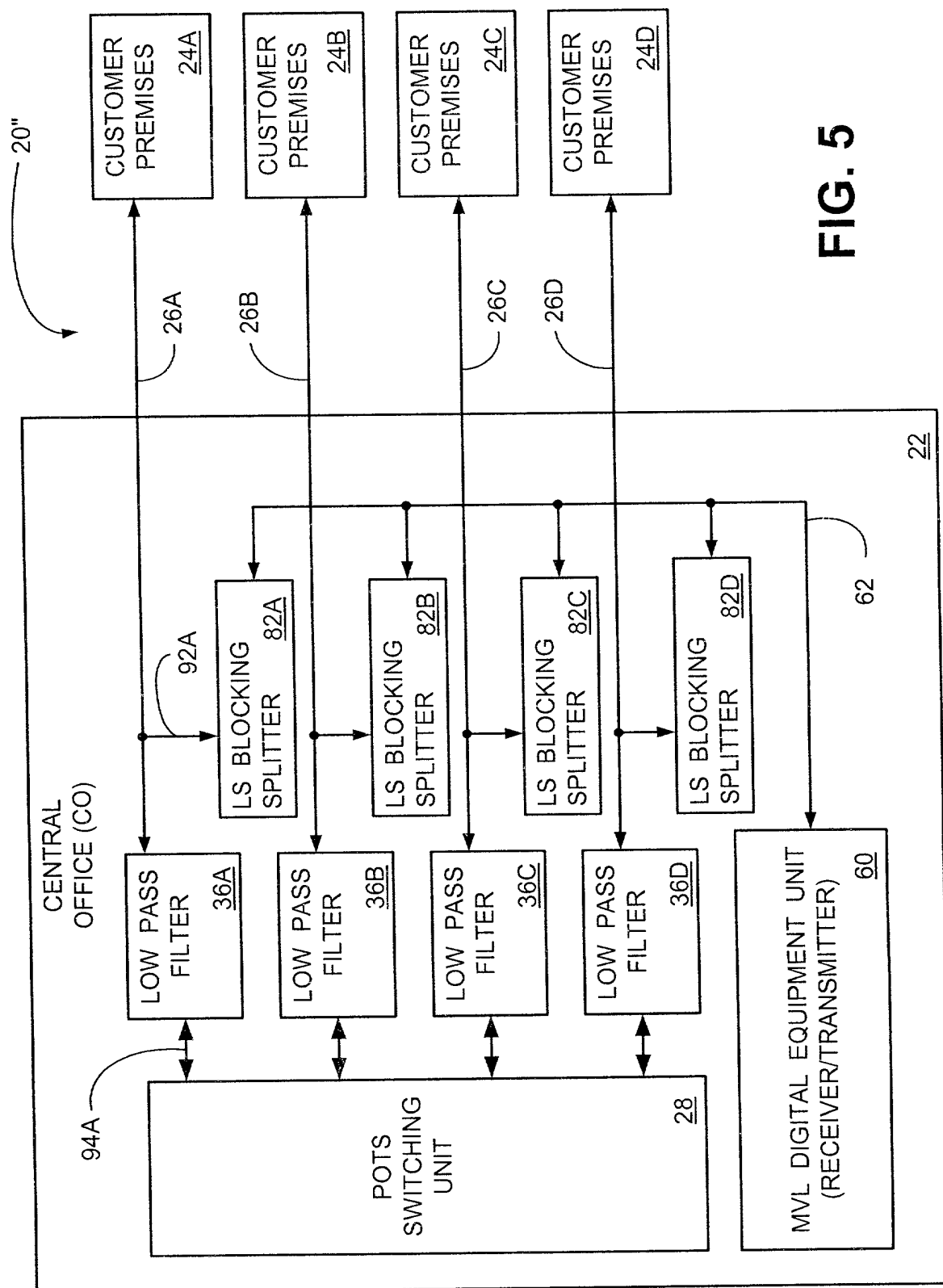


FIG. 5

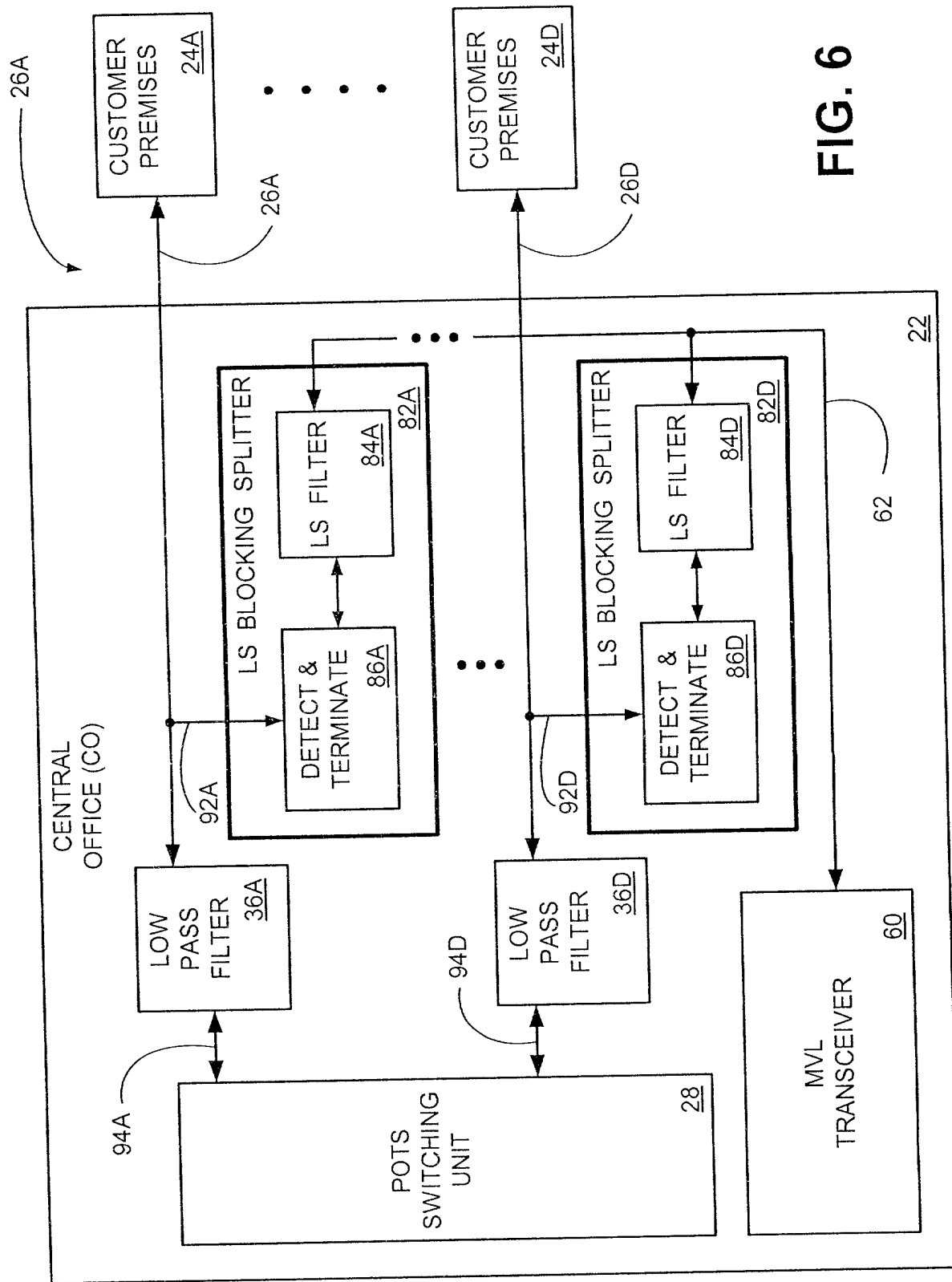
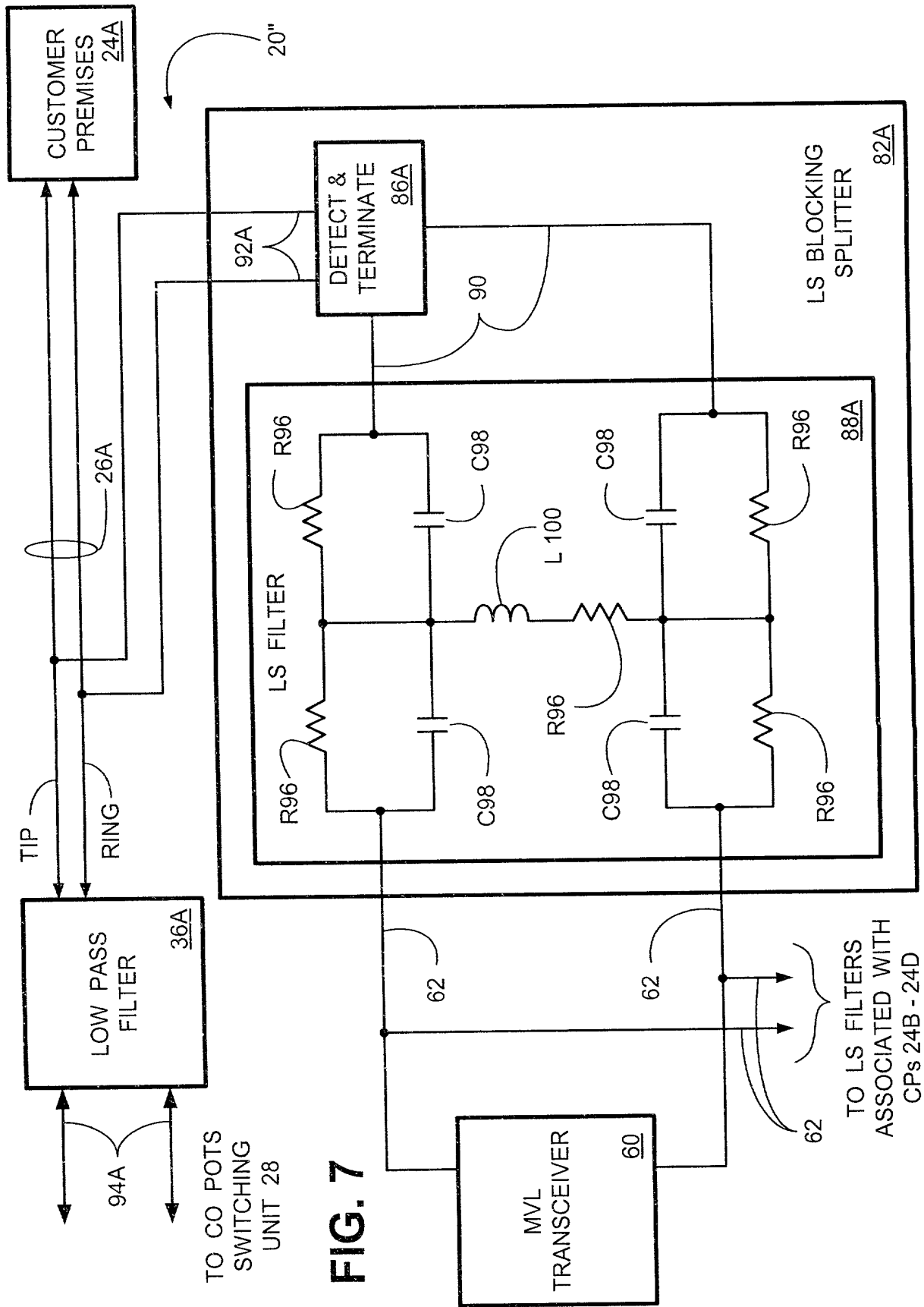


FIG. 6



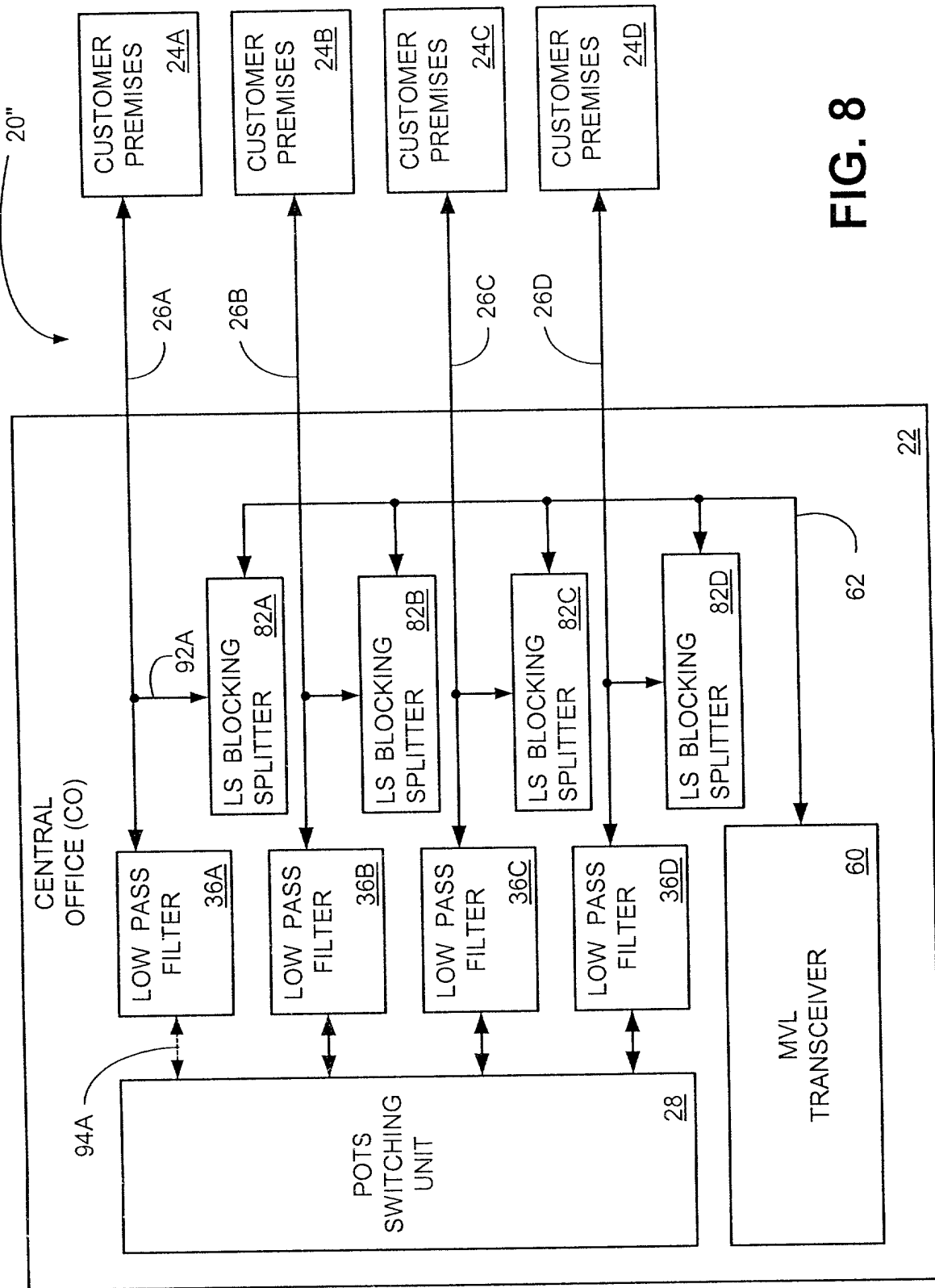


FIG. 8

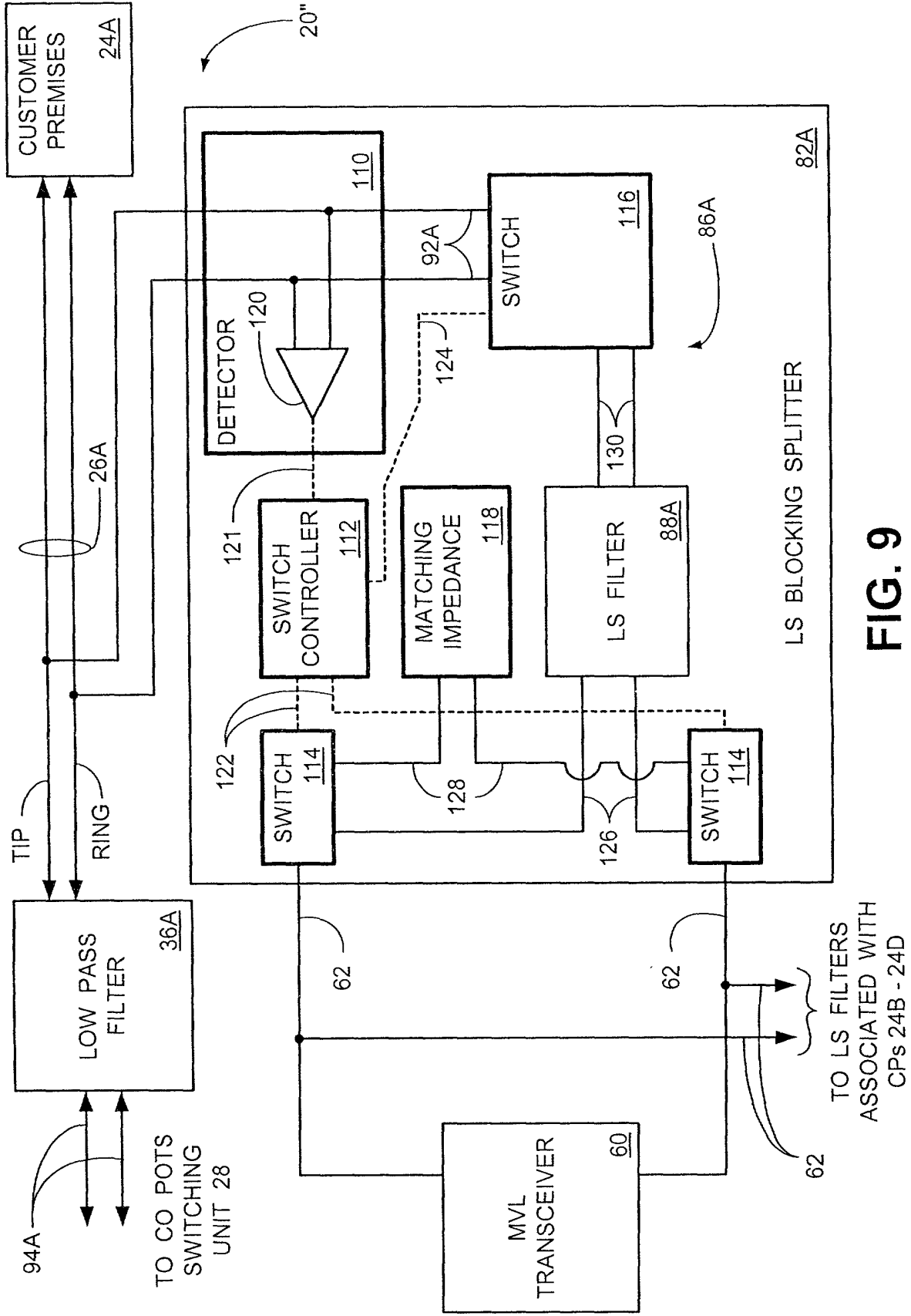


FIG. 9

FIG. 10

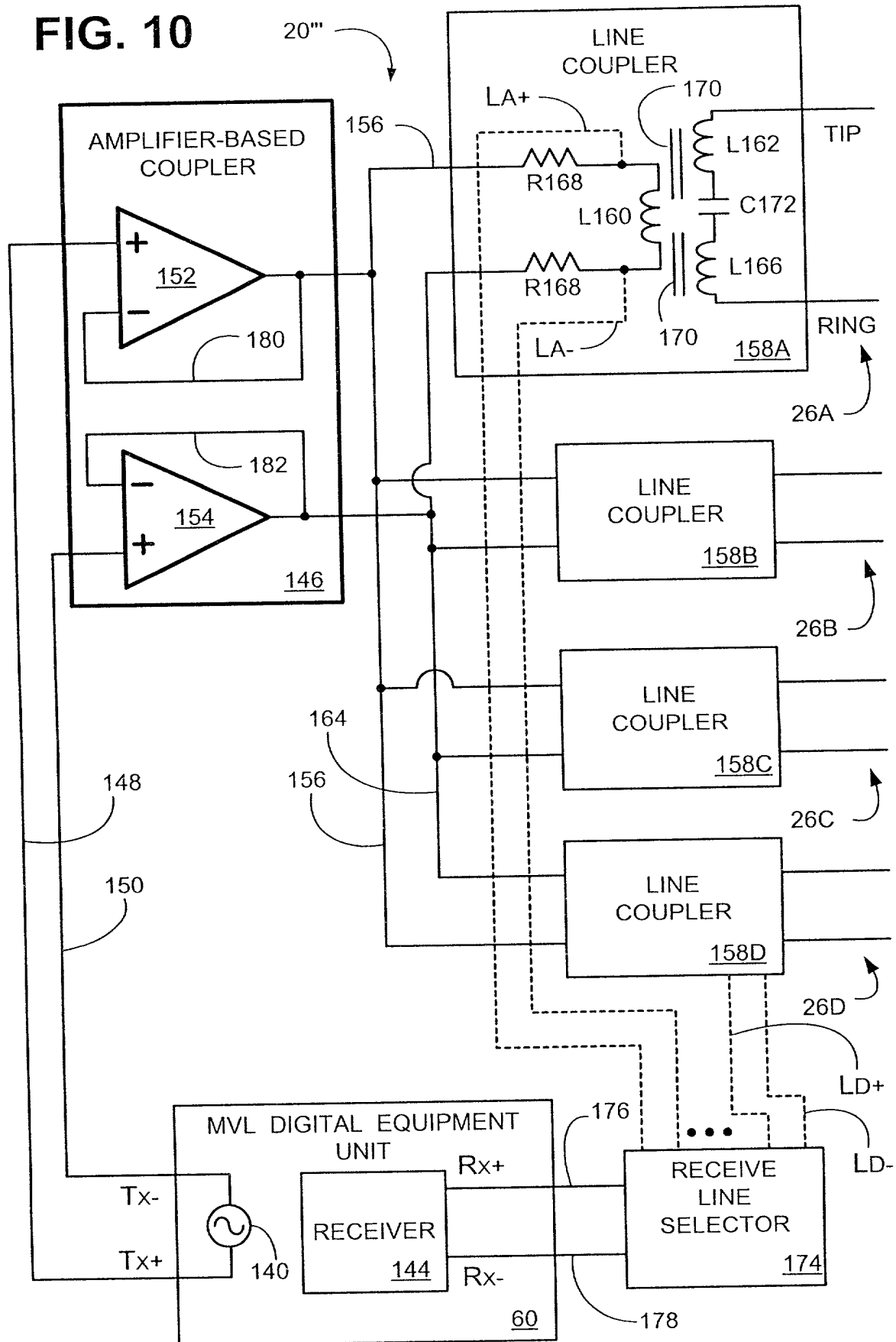


FIG. 11

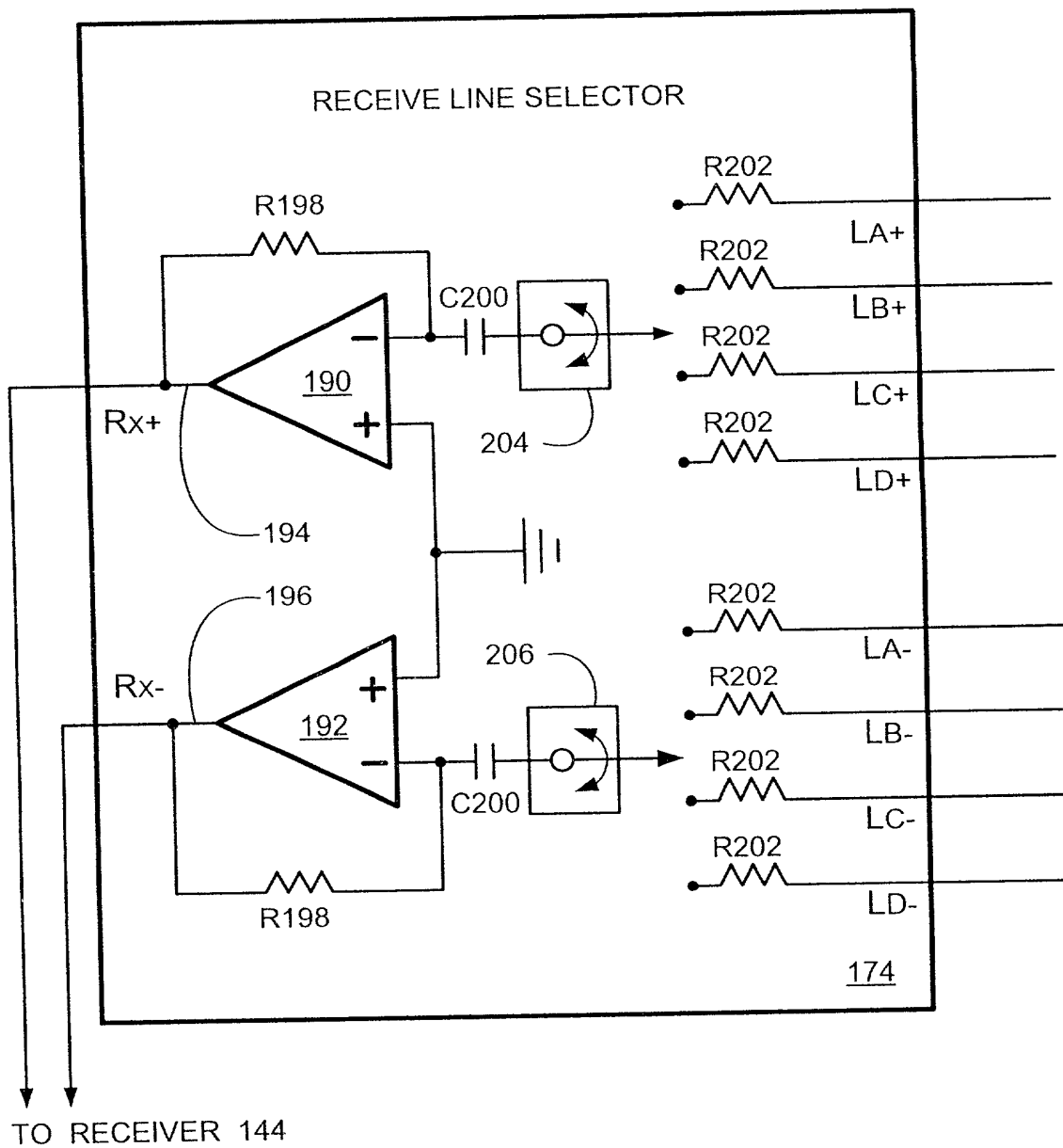
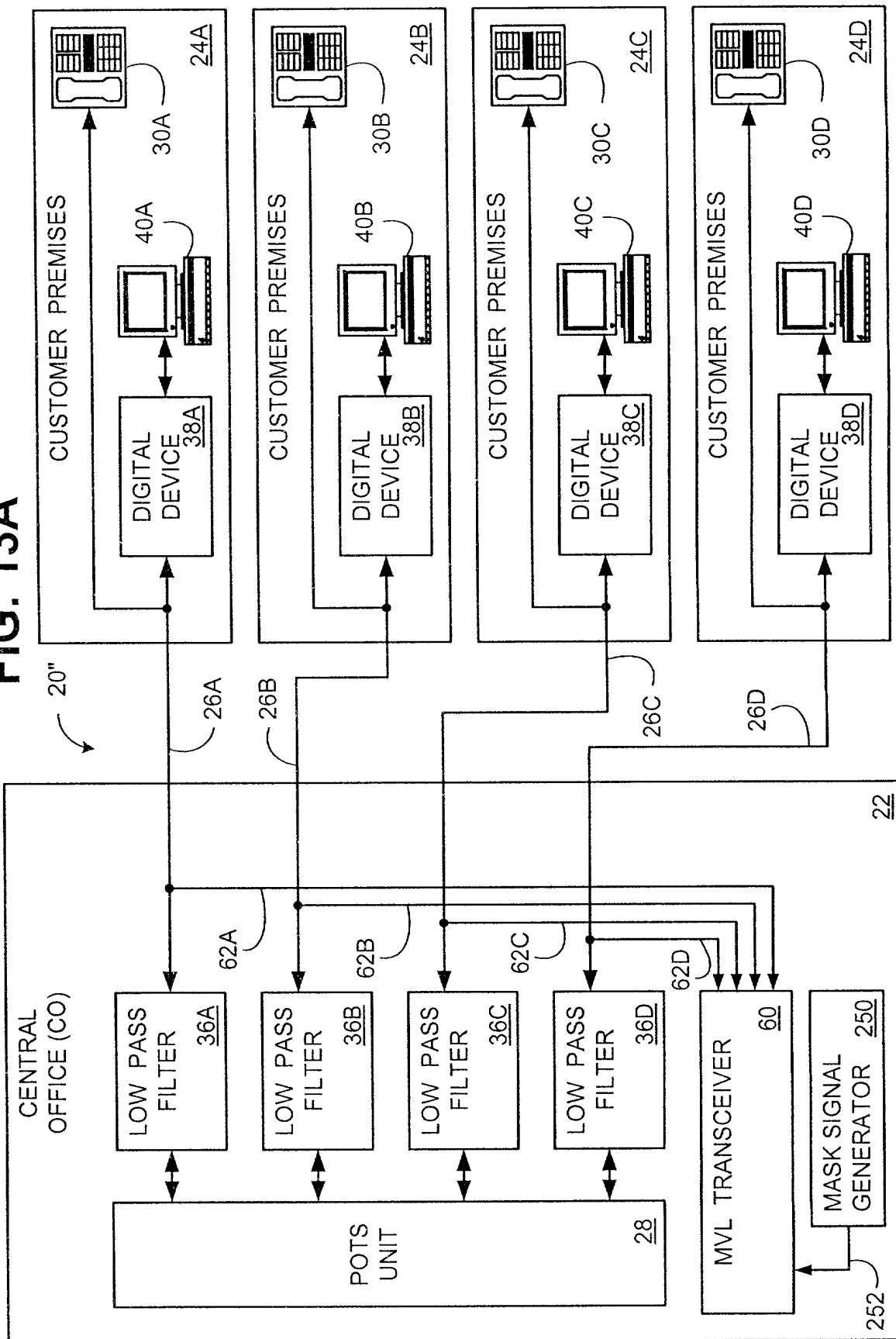


FIG. 13A



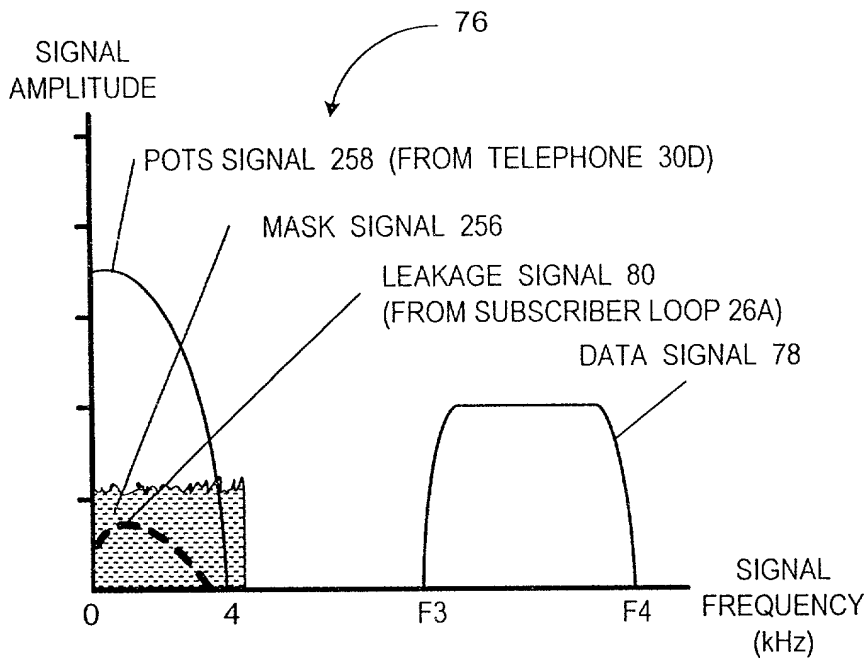


FIG. 14

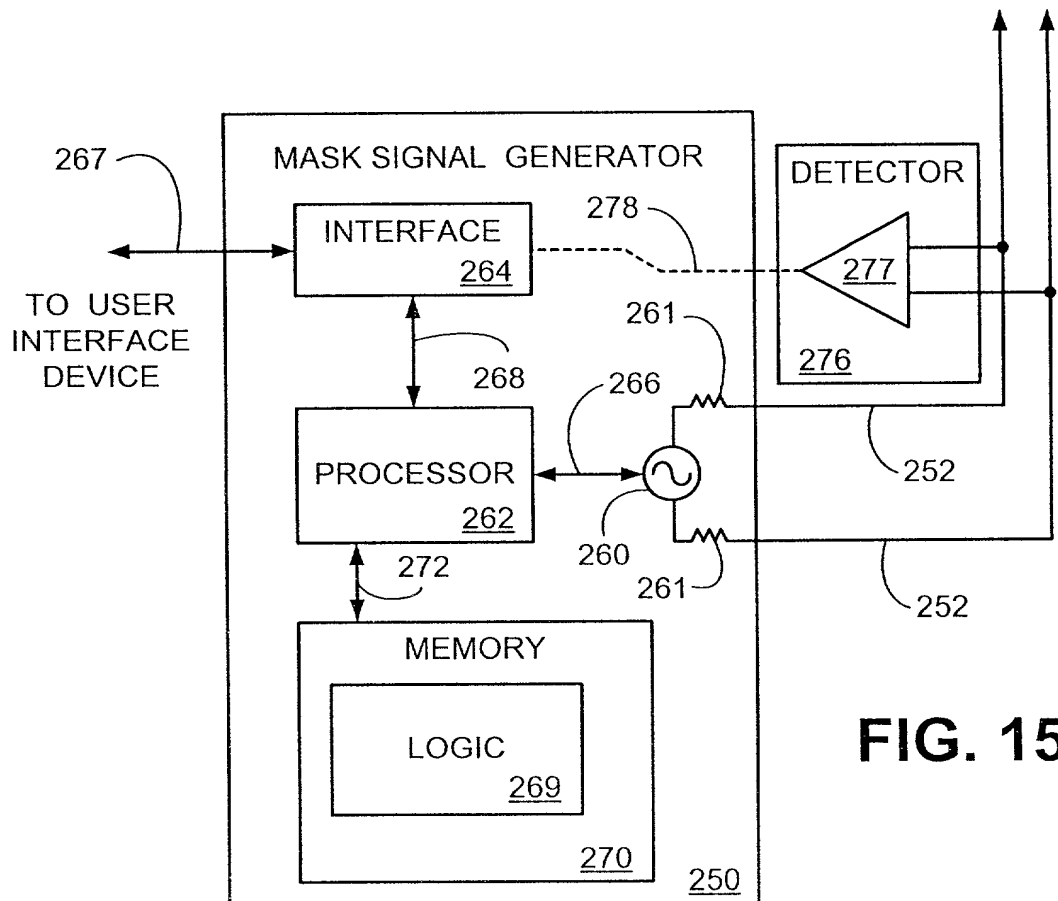


FIG. 15

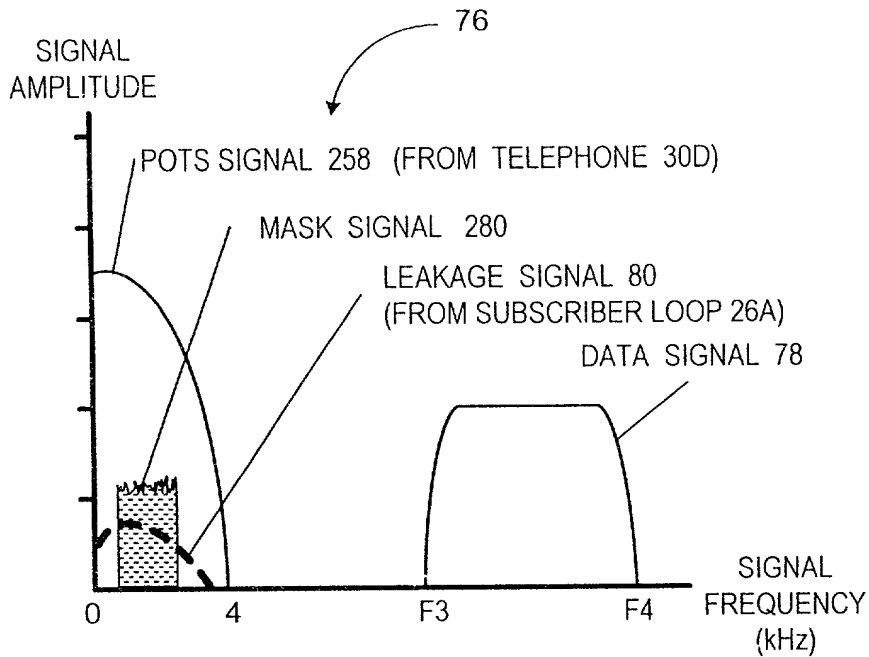


FIG. 16A

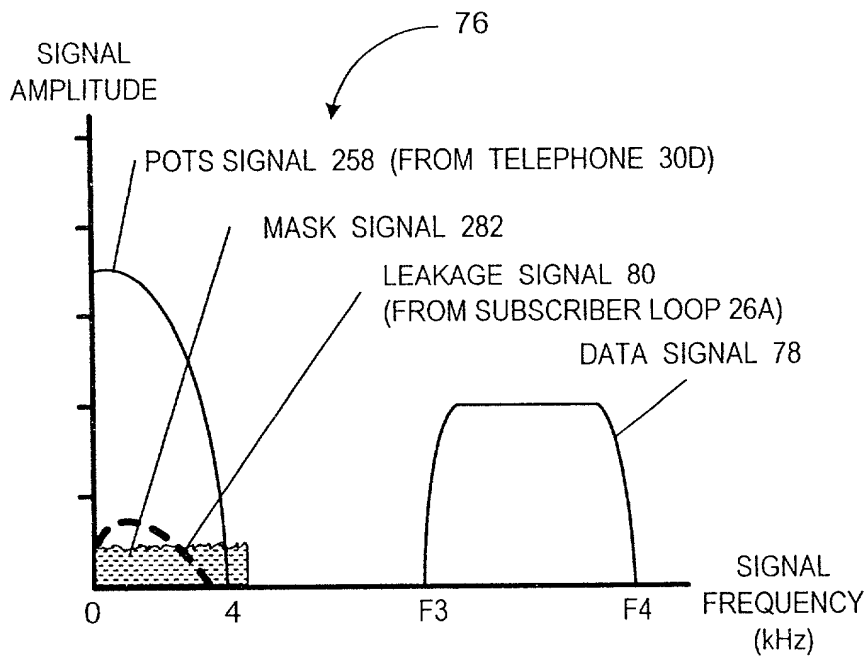


FIG. 16B

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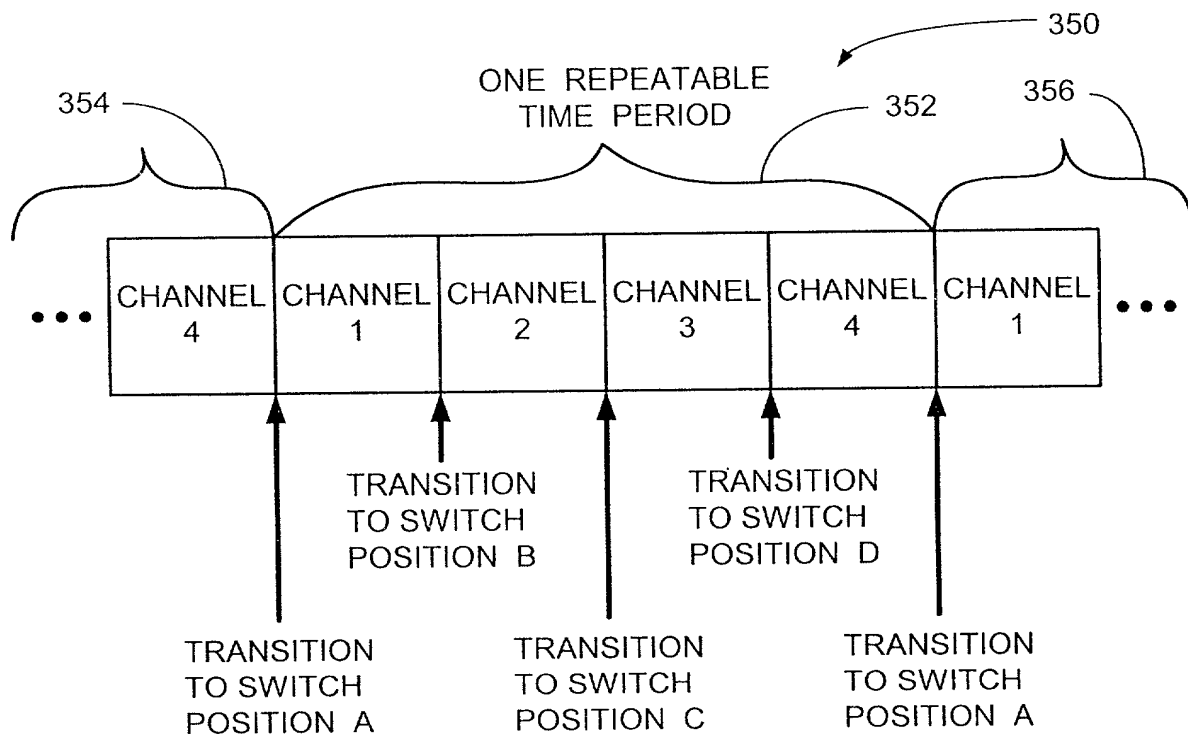
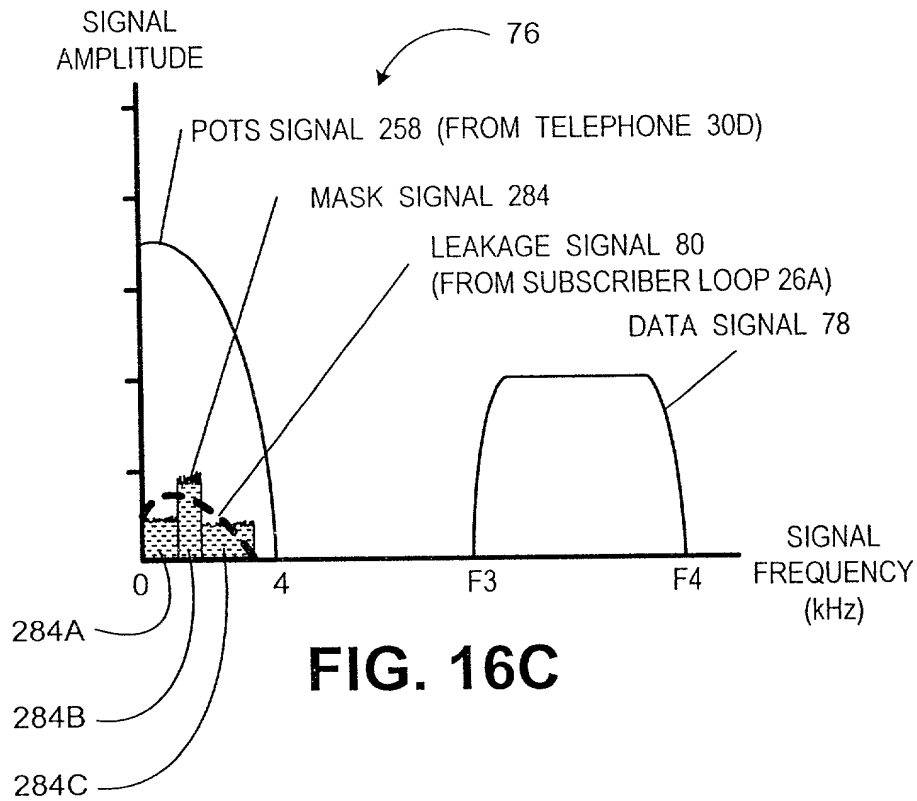


FIG. 18

FIG. 17

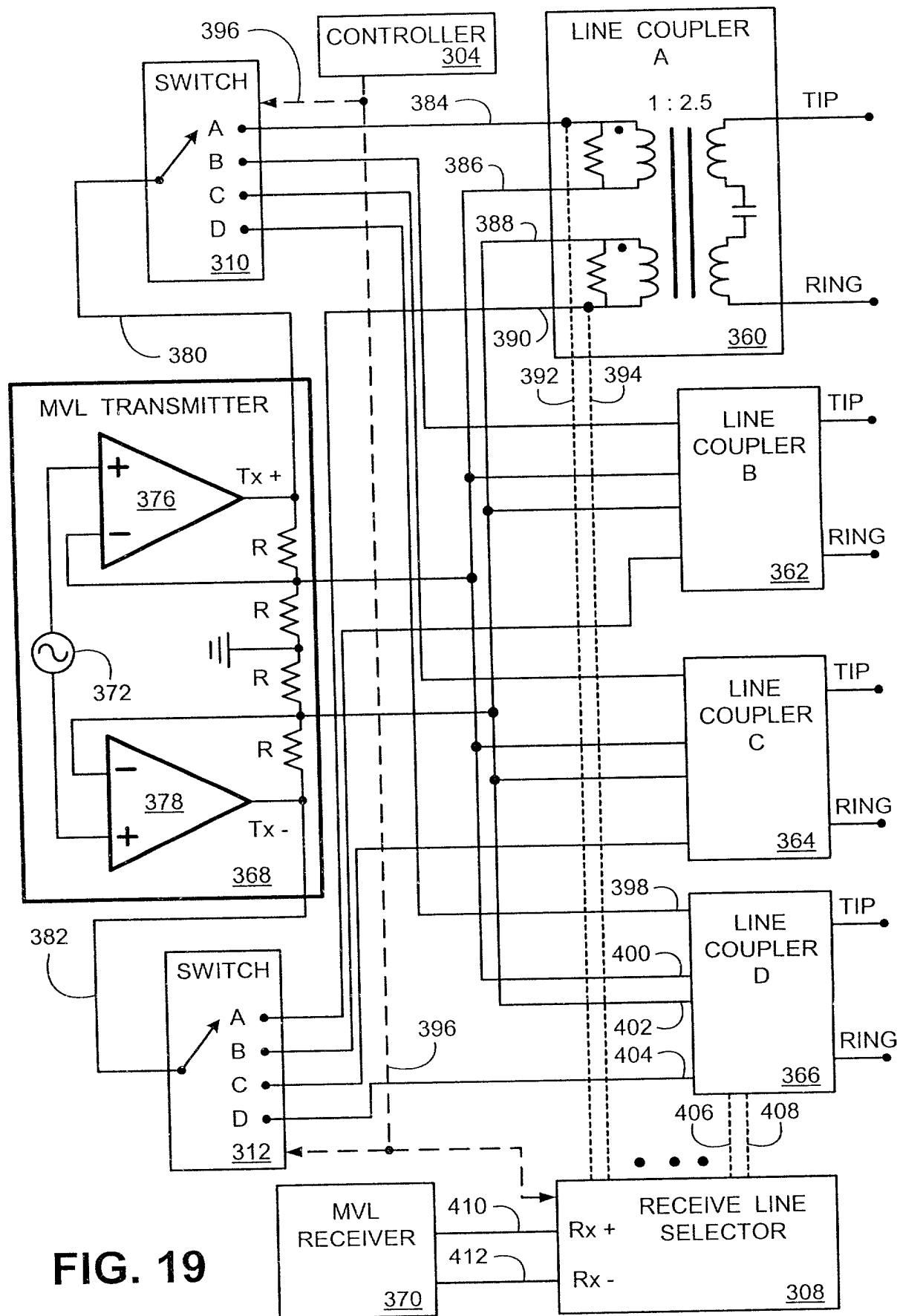


FIG. 19

FIG. 20 is a block diagram of a system architecture. An external device (428) is connected to a controller (304). The controller (304) contains a processor (420) and a logic/memory block (422/426). The processor (420) is connected to the logic/memory block (422/426) via a bidirectional bus (424). The processor (420) also receives inputs (344, 430) and outputs (336, 338, 340, 342) to other components.

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graph TD; START([START]) --> 442[DETERMINE CURRENT CHANNEL 442]; 442 --> 444[READ SWITCH POSITION ASSIGNMENT FOR NEXT CHANNEL 444]; 444 --> 446[DETECT CHANNEL TRANSITION 446]; 446 --> 448[GENERATE CONTROL SIGNAL TO ACTUATE SWITCH TO NEXT ASSIGNED POSITION 448]; 448 --> 450{HAS COMMUNICATION SIGNAL ENDED? 450}; 450 -- YES --> END([END]); 450 -- NO --> 444;
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440

FIG. 21

FIG. 21

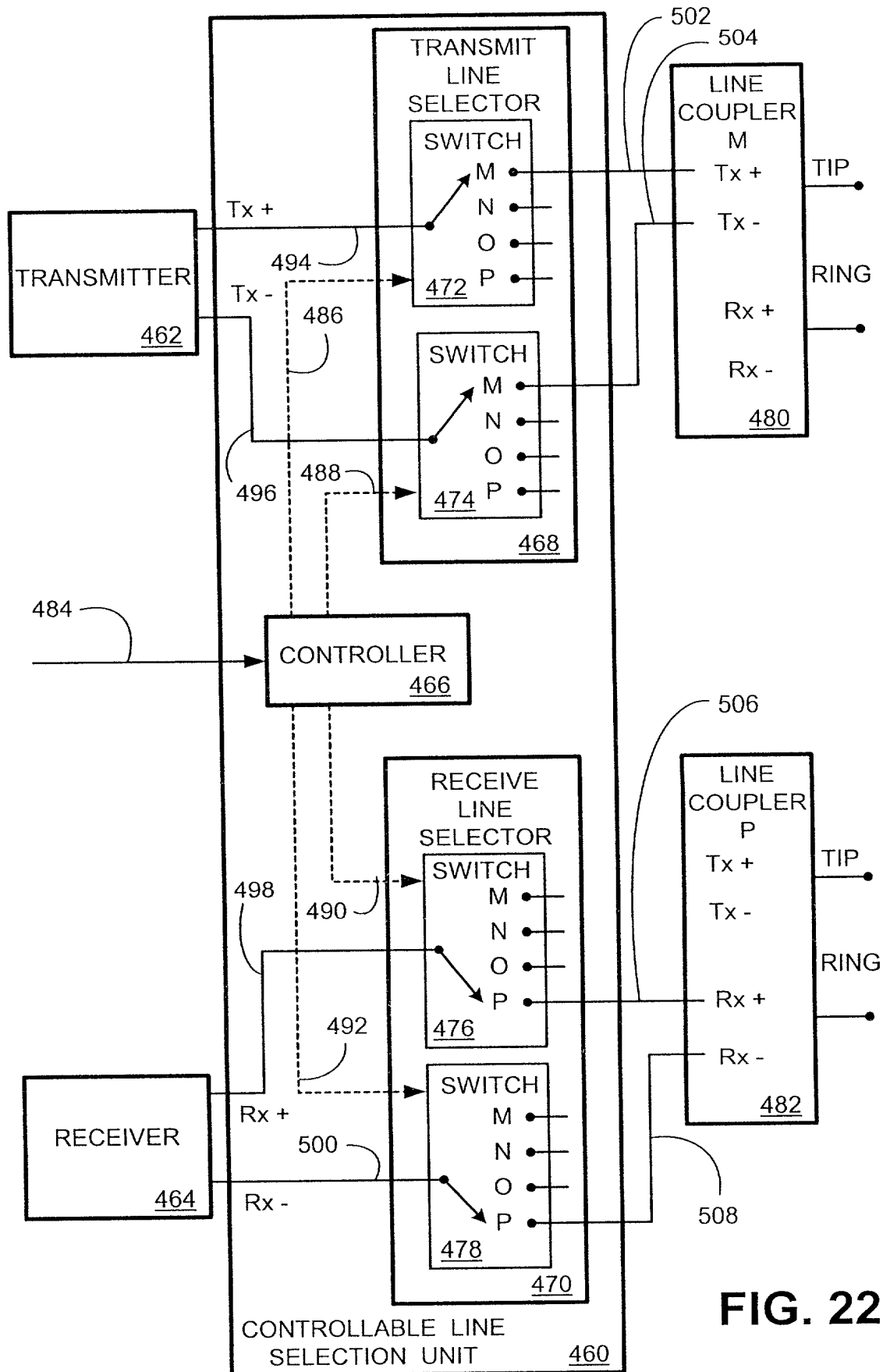


FIG. 22

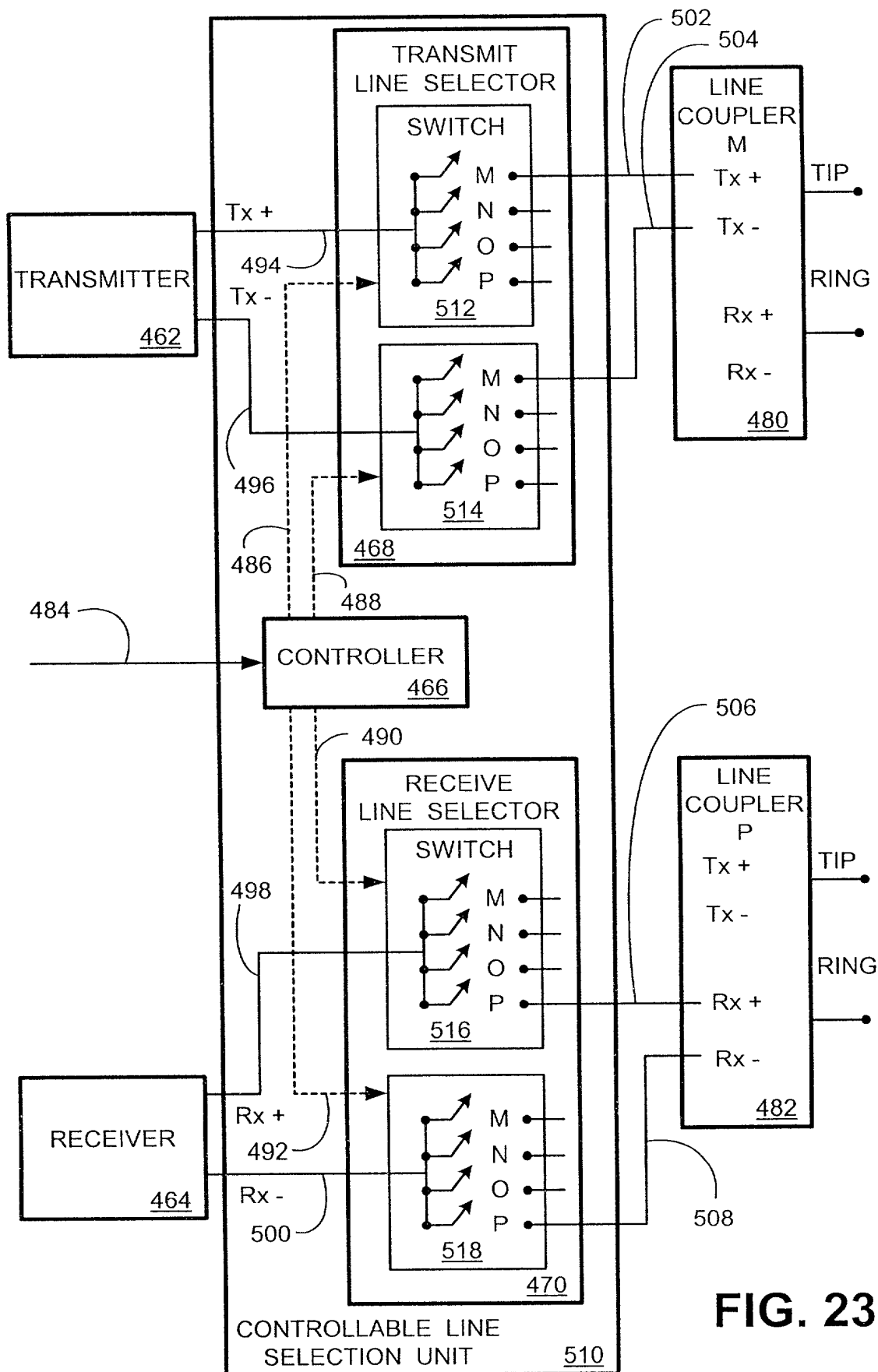


FIG. 23